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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/699,784 | 11/04/2003 | Kuniaki Mamitsu | 01-103-CON7 | 5802 |

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| EXAMINER | |
|---|---|
| WILLIAMS, ALEXANDER O | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2826 | |

DATE MAILED: 11/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/699,784 | MAMITSU ET AL. | |
| | Examiner | Art Unit | |
| | Alexander O Williams | 2826 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *19 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *66-69* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *66-69* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/14; 8/10; 11/4*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/699784 Attorney's Docket #: 01-103-CON7
Filing Date: 11/3/03; claimed foreign priority to 11/24/99(2); 3/24/00; 3/30/00(2); and 10/4/00

Applicant: Mamitsu et al.

Examiner: Alexander Williams

Applicant's election of species of figure 26 (claims 66 to 68), filed 8/19/04, has been acknowledged.

Claims 1-65 have been canceled.

Acknowledgment is made of applicant's claim for foreign priority based on an application filed in Japan on 11/24/99(2); 3/24/00; 3/30/00(2); and 10/4/00. It is noted, however, that applicant has not filed a certified copy of the foreign application as required by 35 U.S.C. 119(b).

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The disclosure is objected to because of the following informalities: For example, on page 74, line 15, "the first cupper foil" should probably be –the first copper foil— and anywhere else throughout the specification.

Appropriate correction is required.

Claims 66 to 69 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 66, it is unclear and confusing to what is meant by and what shows "a silicon semiconductor chip **having an element formation surface** and

**a back surface at an opposite side of the element formation surface**; an electrode formed on the element formation surface of the substrate and made of pure A1 **excluding an impurity**" and "wherein the emitter terminal and the collector terminal are **disposed to face** the gate terminal." Where is this shown in the elected species? Does the element formation surface exist on the surface of the silicon semiconductor chip or substrate; or is there an element region with a surface and back surface?

Claim 66 recites the limitation " a barrier metal disposed between the electrode and **the substrate**" in the semiconductor device. There is insufficient antecedent basis for this limitation in the claim. Applicant claims a semiconductor chip and a substrate.

In claim 68, it is unclear and confusing to what is meant and what shows "comprising **a resin concavity portion** disposed in a direction perpendicular to an extending direction of the emitter terminal, the collector terminal and the gate terminal." Where is this shown in the elected species?

Claim 69 recites the limitation " further comprising a land formed **on the elements formation of the substrate** on the silicon semiconductor chip" in the semiconductor device. There is insufficient antecedent basis for this limitation in the claim. Applicant claims a semiconductor chip and a substrate. Where is this shown in the elected species?

Any of claims 66 to 69 not specifically addressed above are rejected as being dependent on one or more of the claims which have been specifically objected to above.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claims 66 to 69, **insofar as they can be understood**, are rejected under 35 U.S.C. § 103(a) as being unpatentable over Adamic et al. (U.S. Patent # 6,084,284) in view of Etou et al. (U.S. Patent # 5,915,179).

66. Adamic, Jr. (figures 1 to 10) specifically figure 1 show a semiconductor device **112** comprising: a silicon semiconductor chip **(not shown, 108)** having an element formation **110** surface **120** and a back surface **122** at an opposite side of the element formation surface; an electrode **113,154,** formed on the element formation surface of the substrate; a barrier metal **106,105** disposed between the electrode and the substrate, for preventing silicon from being dissolved in the electrode; and an emitter terminal **113 from 620**, a collector terminal **113 from 287** and a gate terminal **113 from 411,412**, wherein the emitter terminal and the collector terminal are disposed to face the gate terminal. Nakamura et al. fail to explicitly show an electrode formed on the element formation surface of the substrate and made of pure Al excluding an impurity.

Etou et al is cited for showing a semiconductor device. Specifically, Etou et al. (figures 1A to 8B) specifically figures 2 and 5A discloses a barrier metal **31**

disposed between the electrode **32,** wherein the electrode **32** is made of pure Al **(see column 3, lines 50-61)** excluding an impurity and the substrate **22** for preventing silicon from being dissolved in the electrode for the purpose of performing switching operation, and achieving various improved characteristics.
67. The semiconductor device of claim 66, the combination with Nakamura et al. show wherein the silicon semiconductor chip is either **a IGBT chip** or a FWD chip.
68. The semiconductor device of claim 66, the combination with Etou et al. further comprising a resin concavity portion disposed in a direction perpendicular to an extending direction of the emitter terminal, the collector terminal and the gate terminal **(see figure 5A and column 10, lines 1-9)**.
69. The semiconductor device of claim 66,the combination with Nakamura et al. further comprising a land **52** formed on the elements formation of the substrate on the silicon semiconductor chip; and metallic film disposed on the electrode and not disposed on the land.

Therefore, it would have been obvious to one of ordinary skill in the art to use Etou et al.'s pure Al electrode to modify Nadamic, Jr.'s electrode for preventing silicon from being dissolved in the electrode for the purpose of performing switching operation, and achieving various improved characteristics.

Claims 66 to 69, **insofar as they can be understood**, are rejected under 35 U.S.C. § 103(a) as being unpatentable over Nakamura et al. (U.S. Patent Application Publication # 2003/0042537 A1) in view of Etou et al. (U.S. Patent # 5,915,179).

66. Nakamura et al. (figures 1 to 56) specifically figure 2 show a semiconductor device comprising: a silicon semiconductor chip **1** having an element formation **2** surface **(top of 1 and bottom of 2)** and a back surface **(top of 2)** at an opposite side of the element formation surface; an electrode **11** formed on the element formation surface of the substrate; a barrier metal **10** disposed between the electrode and the substrate, for preventing silicon from being dissolved in the electrode; and an emitter terminal **11**, a collector terminal **12** and a gate terminal **5a**, wherein the emitter terminal and the collector terminal are disposed to face the gate terminal. Nakamura et al. fail to explicitly show an electrode formed on the element formation surface of the substrate and made of pure Al excluding an impurity.

Etou et al is cited for showing a semiconductor device. Specifically, Etou et al. (figures 1A to 8B) specifically figures 2 and 5A discloses a barrier metal **31** disposed between the electrode **32,** wherein the electrode **32** is made of pure Al **(see column 3, lines 50-61)** excluding an impurity and the substrate **22** for preventing silicon from being dissolved in the electrode for the purpose of performing switching operation, and achieving various improved characteristics.

67. The semiconductor device of claim 66, the combination with Nakamura et al. show wherein the silicon semiconductor chip is either **a IGBT chip** or a FWD chip.
68. The semiconductor device of claim 66, the combination with Etou et al. further comprising a resin concavity portion disposed in a direction perpendicular to an extending direction of the emitter terminal, the collector terminal and the gate terminal **(see figure 5A and column 10, lines 1-9)**.
69. The semiconductor device of claim 66,the combination with Nakamura et al. further comprising a land **52** formed on the elements formation of the substrate on the silicon semiconductor chip; and metallic film disposed on the electrode and not disposed on the land.

Therefore, it would have been obvious to one of ordinary skill in the art to use Etou et al.'s pure Al electrode to modify Nakamura et al.'s electrode for preventing silicon from being dissolved in the electrode for the purpose of performing switching operation, and achieving various improved characteristics.

Applicant cannot rely upon the foreign priority papers to overcome this rejection because a translation of said papers has not been made of record in accordance with 37 CFR 1.55. See MPEP § 201.15.

The listed references are cited as of interest to this application, but not applied at this time.

| Field of Search | Date |
|---|---|
| U.S. Class and subclass:<br>257/486-488,484,139,147,170,173,368,490,328,329,330,<br>506,508,347,773 | 11/2/04 |
| Other Documentation:<br>foreign patents and literature in 257/486-<br>488,484,139,147,170,173,368,490,328,329,330,<br>506,508,347,773 | 11/2/04 |
| Electronic data base(s):<br>U.S. Patents EAST | 11/2/04 |

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alexander O Williams
Primary Examiner
Art Unit 2826

AOW
11/2/04